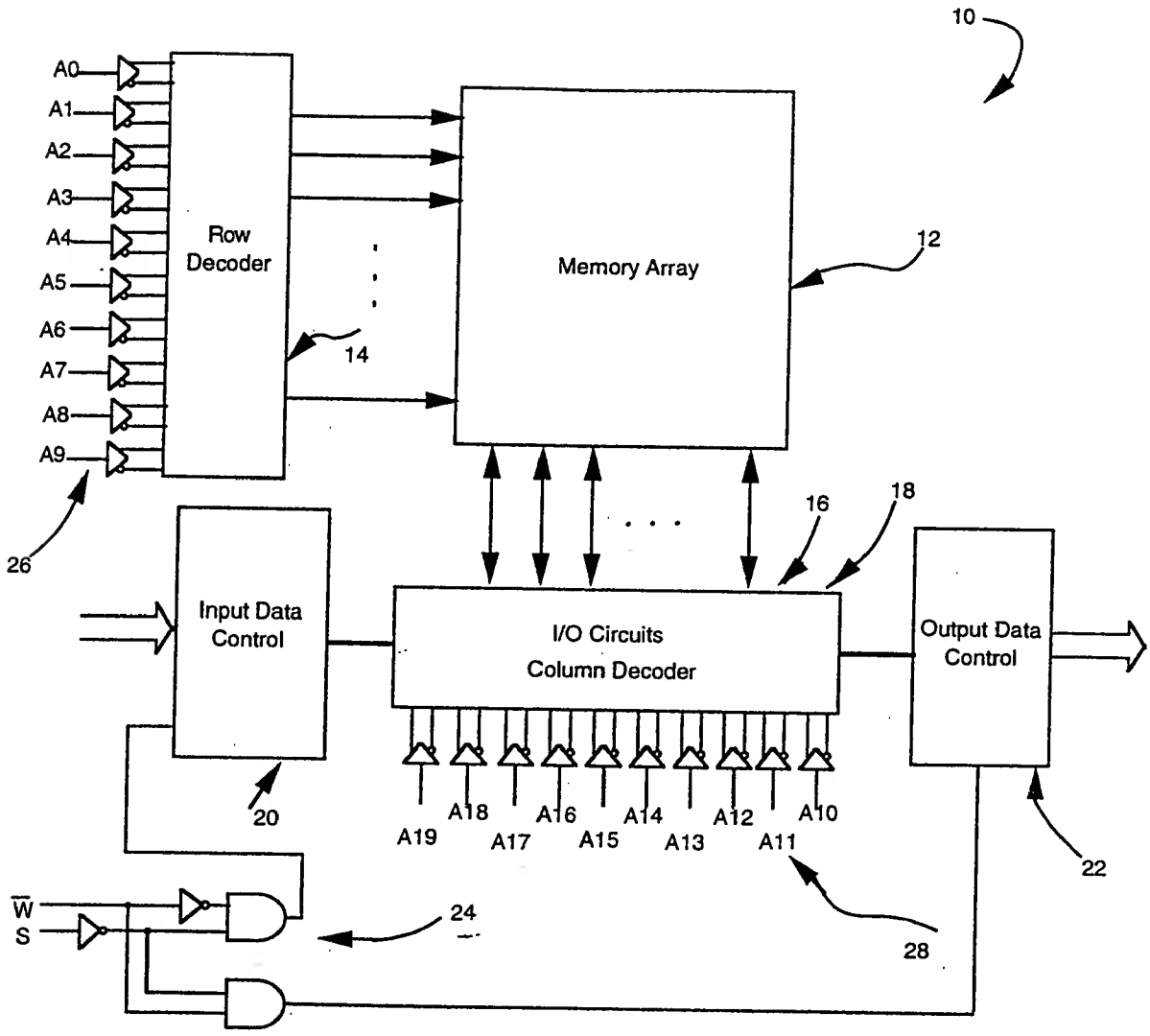
10
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
Row Decoder
14
Memory Array
12
26
16
18
Input Data Control
I/O Circuits Column Decoder
Output Data Control
20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
22
W
S
24
28

FIG. 1

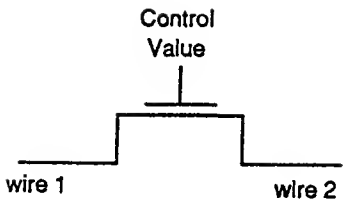

FIG 2A

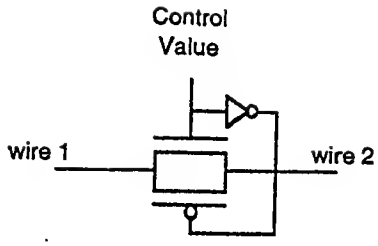

FIG 2B

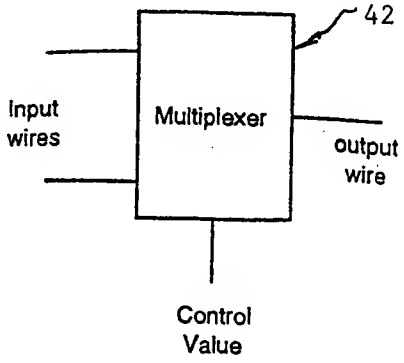

FIG 2C

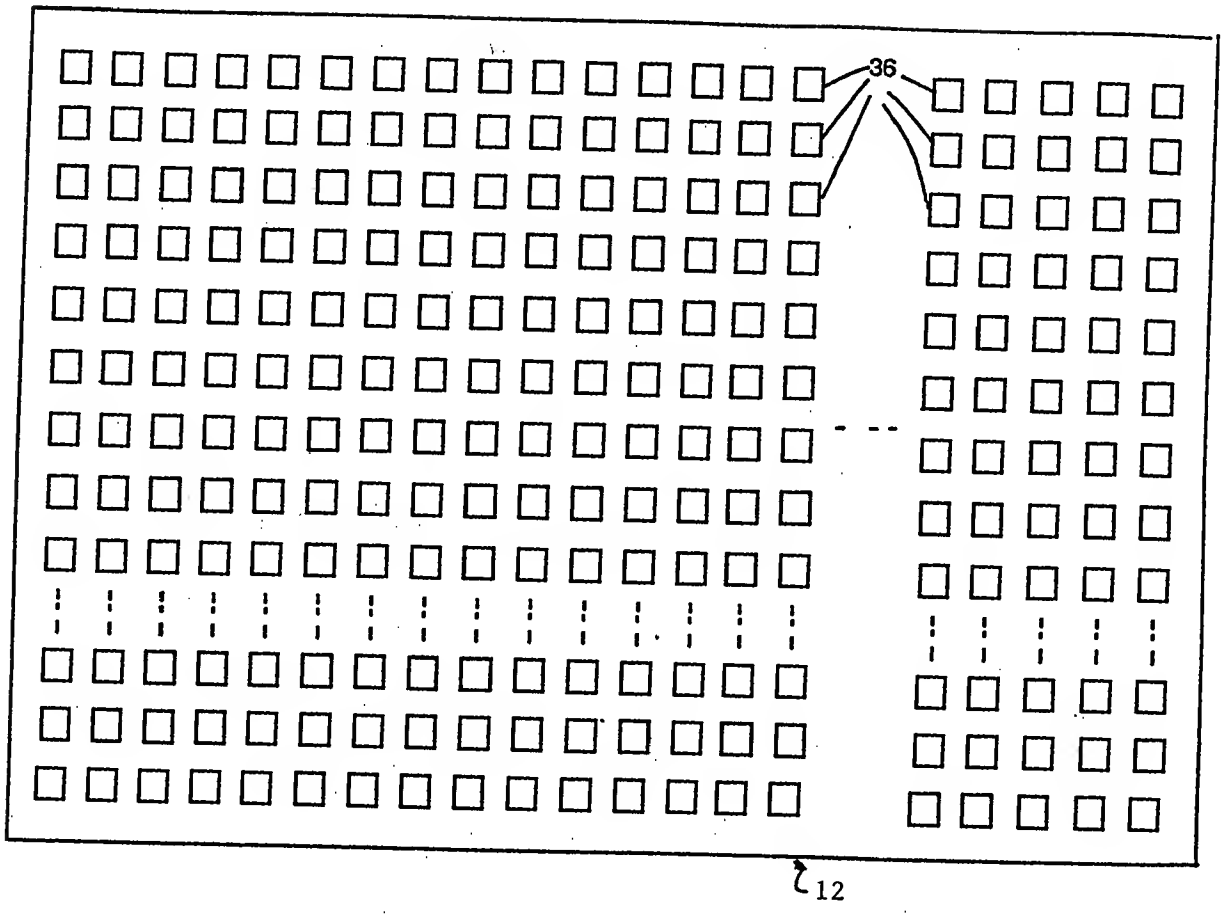

FIG. 3

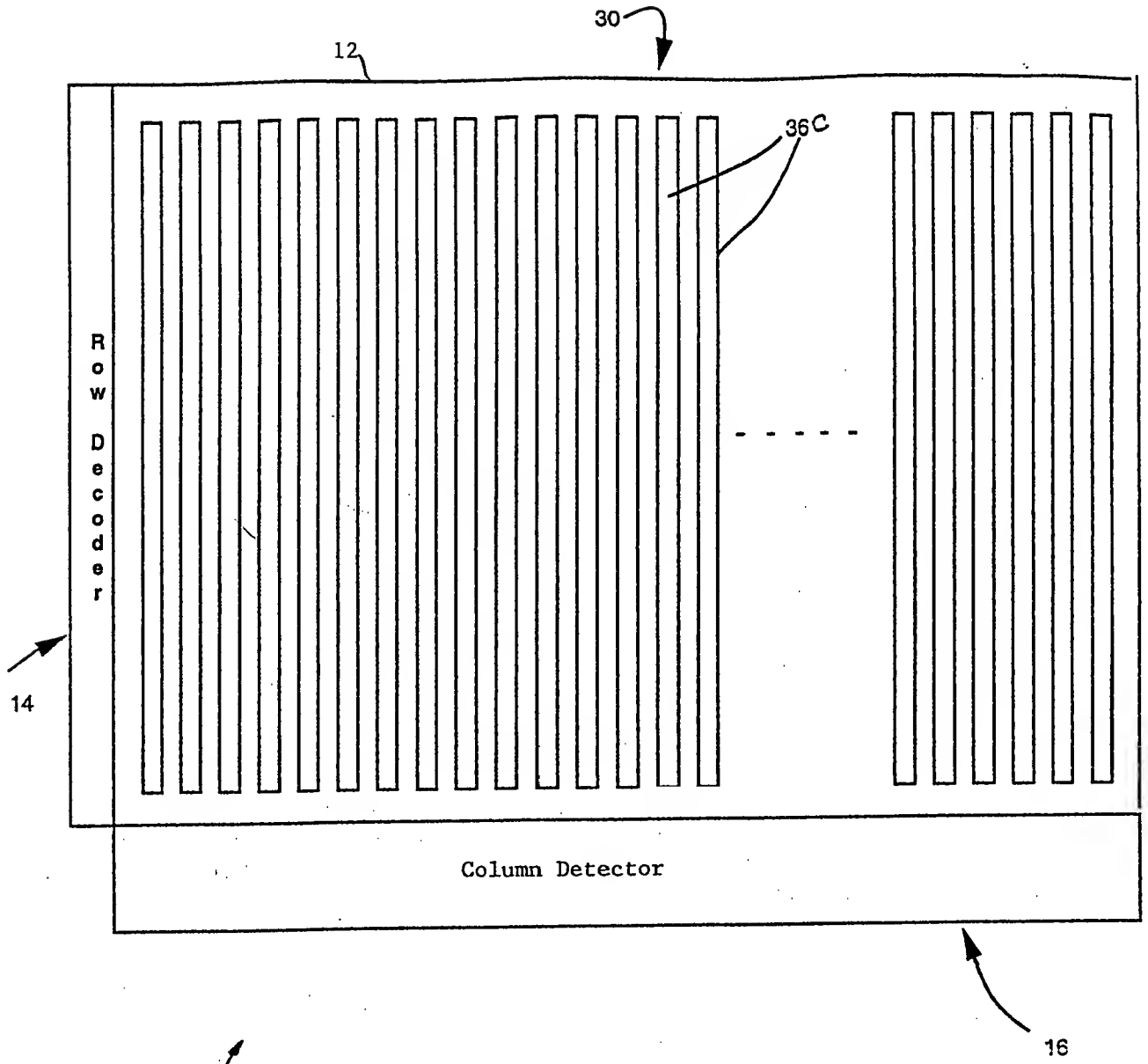

FIG. 4

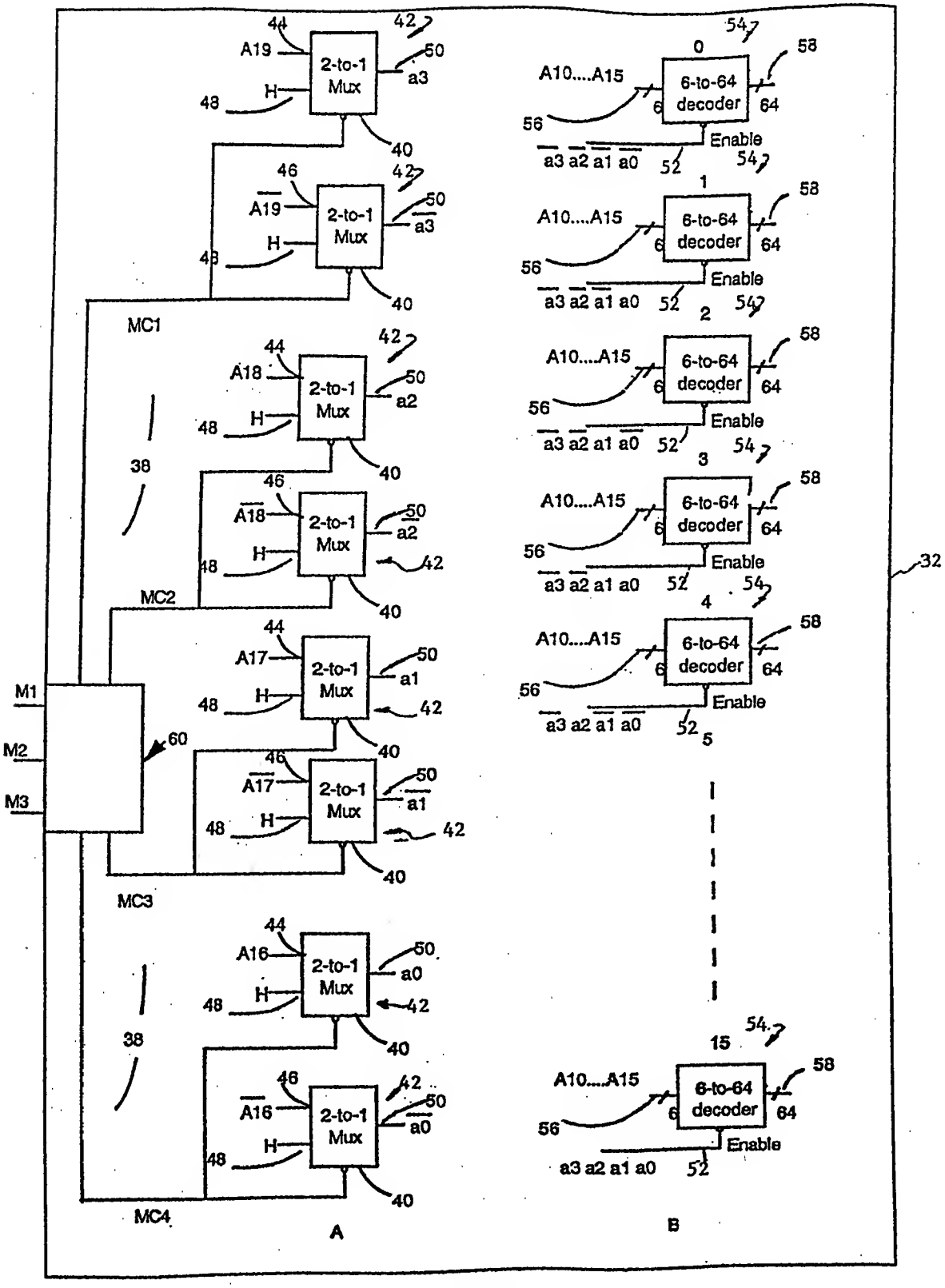
2-to-1 Mux
A19
A18
A17
A16
H
a3
a2
a1
a0
MC1
MC2
MC3
MC4
M1
M2
M3
38
60
A
6-to-64 decoder
A10....A15
Enable
a3 a2 a1 a0
B
32

FIG 5

MC4	MC3	MC2	MC1	a3	a2	a1	a0	$\overline{a3}$	$\overline{a2}$	$\overline{a1}$	$\overline{a0}$	Configuration
1	1	1	1	A19	A18	A17	A16	$\overline{A19}$	$\overline{A18}$	$\overline{A17}$	$\overline{A16}$	1 bit wide
1	1	1	0	H	A18	A17	A16	H	$\overline{A18}$	$\overline{A17}$	$\overline{A16}$	2 bit wide
1	1	0	0	H	H	A17	A16	H	H	$\overline{A17}$	$\overline{A16}$	4 bit wide
1	0	0	0	H	H	H	A16	H	H	H	$\overline{A16}$	8 bit wide
0	0	0	0	H	H	H	H	H	H	H	H	16 bit wide

FIG. 6

M3	M2	M1	MC4	MC3	MC2	MC1
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	1	1	0	0
0	1	1	1	1	1	0
1	0	0	1	1	1	1

FIG 7

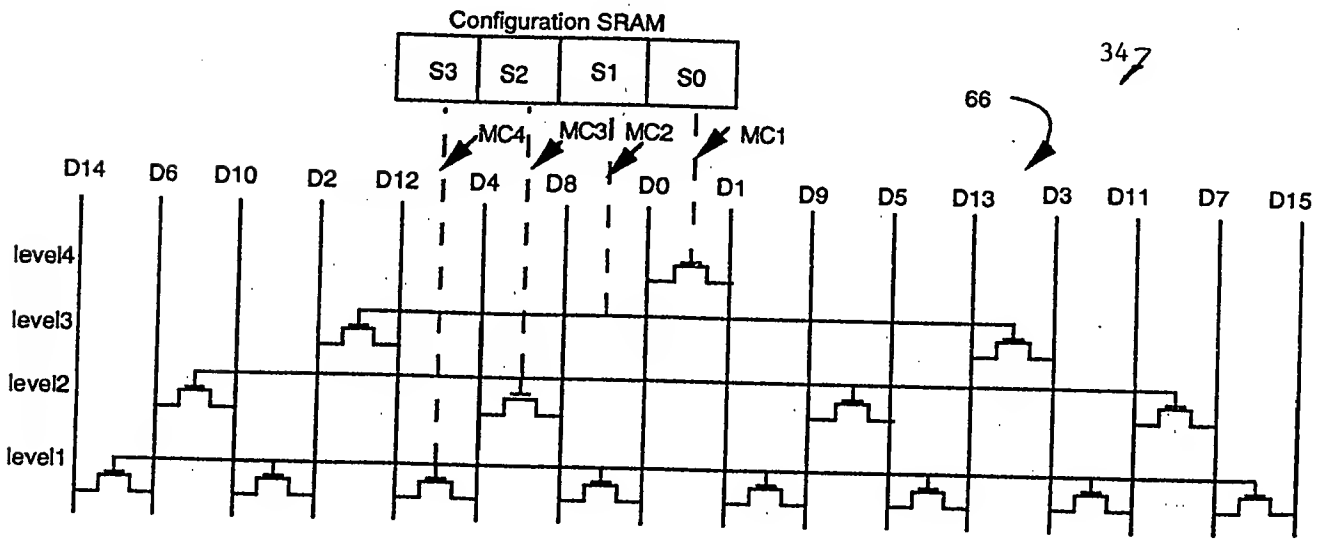

FIG 8

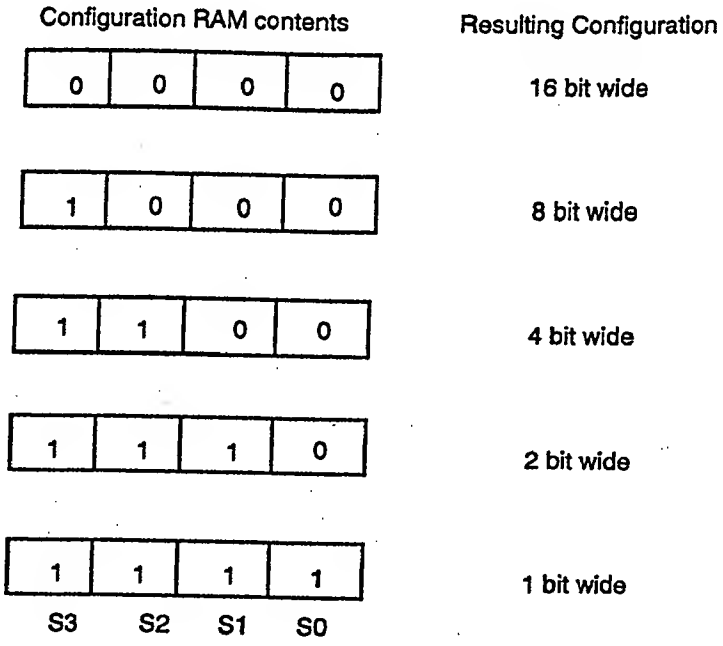
Configuration RAM contents
Resulting Configuration
0 0 0 0
16 bit wide
1 0 0 0
8 bit wide
1 1 0 0
4 bit wide
1 1 1 0
2 bit wide
1 1 1 1
1 bit wide
S3 S2 S1 S0

FIG. 9

M	A19	A18	A17	A16	MC4	MC3	MC2	MC1	Configuration
0	x	x	x	x	1	1	1	1	1 bit wide
1	0	x	x	x	1	1	1	0	2 bit wide
1	1	0	x	x	1	1	0	0	4 bit wide
1	1	1	0	x	1	0	0	0	8 bit wide
1	1	1	1	x	0	0	0	0	16 bit wide

FIG. 10